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L8 and L9	53

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L10

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Search History

DATE: Tuesday, December 23, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L10	l8 and l9	53	L10
L9	eeprom or ((nonvolatile or flash) adj memory)	105309	L9
L8	l4 and l6	267	L8
L7	l4 and lL6	0	L7
L6	l1 same l2	1654	L6
L5	l3 and L4	572	L5
L4	711/$.ccls.	19184	L4
L3	l1 and L2	3426	L3
L2	data near2 buffer	87139	L2
L1	command near2 buffer	5618	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Generate Collection Print

L10: Entry 20 of 53 File: USPT Dec 12, 2000

DOCUMENT-IDENTIFIER: US 6161162 A
** See image for Certificate of Correction **
TITLE: Multiprocessor system for enabling shared access to a memory

Brief Summary Text (7):
In some known systems a separate non-volatile storage device is used for each of the multiple processors which increases the cost of the computer system. One method frequently used is to simply employ single chip microcomputers with on-chip memory for the light duty housekeeping chores. This on-chip memory is typically either ROM or EEPROM, both requiring a system disassembly to upgrade the firmware code contained in the memory. The need for multiple non-volatile storage devices in computer systems also adds to the cost of such systems.

Detailed Description Text (33):
The CPU can either write data or a command to the input buffer register 30. Any time the CPU writes to the input buffer 30, a command data flag (CMD/DATA) is set in the status register 34 (bit 3). This lets the SCP 26 know that a byte containing either a command or data is in the input buffer 30. A write to 64H represents a command (command data flag high), while a write to 60H represents data (command data flag low).

L10: Entry 8 of 53 File: USPT May 20, 2003

DOCUMENT-IDENTIFIER: US 6567335 B1
TITLE: Memory system having flexible bus structure and method

Detailed Description Text (4):
The memory devices 38A, 38B and 38C are preferably separate integrated circuits utilizing non-volatile memory technology. The exemplary embodiment will be described using flash memory technology, that being the preferred memory technology. Each Memory Device 38A, 38B, and 38C is capable of storing a substantial amount of data such as forty Megabits. Several memory devices can be added to the memory system to increase the storage capacity.

Detailed Description Text (63):
FIG. 9 is a simplified diagram of the organization of an exemplary flash memory array for use on a single one of the Memory Devices 38. The total capacity of the array is 40 Megabits. The array has a total of ten Main Blocks, each having a capacity of four Megabits, which are addressed using addresses A.sub.22 -A.sub.19. Each four Megabit Main Block is made up of eight 512k bit Erase Blocks which are addressed using addresses A.sub.18 -A.sub.16. The Erase Blocks have separate common source line which permit the Erase Blocks to be separately erased. Continuing, each Erase Block consists of 128 Sectors, with each Sector storing 4352 bits. The Sectors are addressed using addresses A.sub.15 -A.sub.9. Finally, each Sector consists of 17 Packets, with the Packets being addressed by A.sub.8 -A.sub.5, A.sub.x. Address A.sub.x is used to decode the 17th packet, with the 17th packet typically containing certain overhead bits such as error correction codes and the like.

Detailed Description Text (93):
As is well known, flash memory cells have threshold voltages which vary depending upon whether the cell is in an erased state or a programmed state. The threshold voltage is typically defined as the control gate to source voltage across the cell necessary for the cell to conduct one microampere of current for a drain voltage of +1 volt. An erased cell has a relatively low threshold voltage (V.sub.THE), +3 volts for example, and a programmed cell has a relatively high threshold voltage (V.sub.THP), +5 volts, for example. In a read operation, the memory system will operate to ground the source of the cell being read and will apply an appropriate voltage to the control gate by way of the associated Word Line. The drain of the cell, which is connected to the associated Bit Line, is typically set to a small positive voltage such as +1 volt. If the cell has been programmed, the current through the cell will be relatively small and if the cell is in an erased state the current will be relatively high.

Current US Cross Reference Classification (3):
711/100

Current US Cross Reference Classification (4):
711/5

CLAIMS:

h e b b g e e e f c e b g e ge

19. The memory system of claim 13, wherein the memory operation manager includes a command input buffer connected between the tag bus and the command decoder for temporary storage of the memory read address command and a data input buffer connected between the data bus and the array for temporary storage of the memory read address.

29. The memory system of claim 21, wherein the memory operation manager includes a command input buffer connected between the tag bus and the command decoder for temporary storage of the memory data command and a data input buffer connected between the data bus and the array for temporary storage of the memory address.

32. The memory system of claim 31, wherein the memory operation manager includes a command input buffer connected between the first bus and the command decoder for temporary storage of one of first memory program address command and the second memory program address command, and a data input buffer connected between the second bus and the array for temporary storage of one of the first memory address and the second memory address.